12-Bit Serial Input Multiplying CMOS D/A Converter

DAC8043

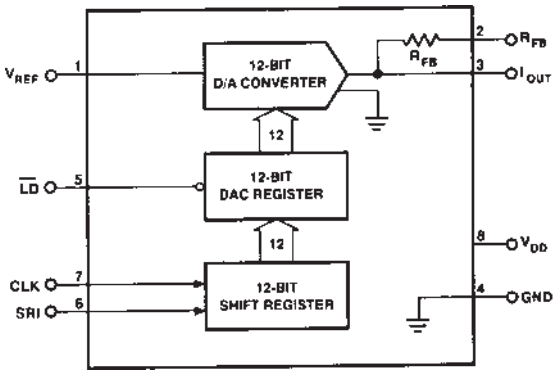
FEATURES

12-Bit Accuracy in an 8-Lead PDIP Package
Fast Serial Data Input
Double Data Buffers
Low ±1/2 LSB Max INL and DNL
Max Gain Error: ±1 LSB
Low 5 ppm/°C Max Tempco
ESD Resistant
Low Cost
Available in Die Form

APPLICATIONS

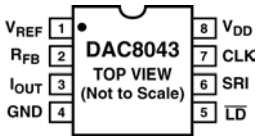
Autocalibration Systems
Process Control and Industrial Automation
Programmable Amplifiers and Attenuators
Digitally Controlled Filters

FUNCTIONAL BLOCK DIAGRAM



PIN CONNECTIONS

8-Lead PDIP



GENERAL DESCRIPTION

The DAC8043 is a high accuracy 12-bit CMOS multiplying DAC in a space-saving 8-lead PDIP package. Featuring serial data input, double buffering, and excellent analog performance, the DAC8043 is ideal for applications where PC board space is at a premium. In addition, improved linearity and gain error performance permit reduced parts count through the elimination of trimming components. Separate input clock and load DAC control lines allow full user control of data loading and analog output.

The circuit consists of a 12-bit serial-in, parallel-out shift register, a 12-bit DAC register, a 12-bit CMOS DAC, and control logic. Serial data is clocked into the input register on the rising edge of the CLOCK pulse. When the new data word has been clocked in, it is loaded into the DAC register with the $\overline{LD}$ input pin. Data in the DAC register is converted to an output current by the D/A converter.

The DAC8043's fast interface timing may reduce timing design considerations while minimizing microprocessor wait states. For applications requiring an asynchronous CLEAR function or more versatile microprocessor interface logic, refer to the PM-7543.

Operating from a single 5 V power supply, the DAC8043 is the ideal low power, small size, high performance solution to many application problems. It is available in a PDIP package that is compatible with auto-insertion equipment.

REV. D

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DAC8043–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

(@ V_{DD} = +5 V; V_{REF} = +10 V; I_{OUT} = GND = 0 V; T_A = Full Temperature Range specified under Absolute Maximum Ratings, unless otherwise noted.)

Parameter	Symbol	Conditions	DAC8043 Min	DAC8043 Typ	DAC8043 Max	Unit
STATIC ACCURACY						
Resolution	N		12			Bits
Nonlinearity[1]	INL	DAC8043G			±1/2	LSB
		DAC8043F			1	LSB
Differential Nonlinearity[2]	DNL	DAC8043F/G			±1	LSB
Gain Error[3]	G_{FSE}	T_A = 25°C				
		DAC8043F/G			2	LSB
		T_A = Full Temperature Range				
		All Grades			2	LSB
Gain Tempco						
(Δ Gain/Δ Temp)[4]	TC_{GFS}				±5	ppm/°C
Power Supply						
Rejection Ratio	PSRR	ΔV_{DD} = ±5%		±0.0006	±0.002	%/%
(Δ Gain/Δ V_{DD})						
Output Leakage Current[5]	I_{LKG}	T_A = 25°C			±5	nA
		T_A = Full Temperature Range				
		DAC8043F/G			±25	nA
Zero Scale Error[6, 7]	I_{ZSE}	T_A = 25°C			0.03	LSB
		T_A = Full Temperature Range				
		DAC8043F/G			0.15	LSB
Input Resistance[8]						
	R_{IN}		7	11	15	kΩ
AC PERFORMANCE						
Output Current						
Settling Time[4, 9]	t_S	T_A = 25°C		0.25	1	µs
		V_{REF} = 0 V				
Digital to Analog		I_{OUT} Load = 100 Ω				
Glitch Energy[4, 10]	Q	C_{EXT} = 13 pF		2	20	nVs
		DAC Register Loaded Alternately with				
		All 0s and All 1s				
Feedthrough Error		V_{REF} = 20 V p-p @ f = 10 kHz				
(V_{REF} to I_{OUT})[4, 11]	FT	Digital Input = 0000 0000 0000		0.7	1	mV p-p
		T_A = 25°C				
Total Harmonic Distortion[4]	THD	V_{REF} = 6 V rms @ 1 kHz		–85		dB
		DAC Register Loaded with All 1s				
Output Noise Voltage Density[4, 12]	e_n	10 Hz to 100 kHz between R_{FB} and I_{OUT}			17	nV/$\sqrt{\text{Hz}}$
DIGITAL INPUTS						
Digital Input						
HIGH	V_{IN}		2.4			V
Digital Input						
LOW	V_{IL}				0.8	V
Input Leakage Current[13]	I_{IL}	V_{IN} = 0 V to +5 V			±1	µA
Input Capacitance[4, 11]	C_{IN}	V_{IN} = 0 V			8	pF
ANALOG OUTPUTS						
Output Capacitance[4]	C_{OUT}	Digital Inputs = V_{IH}			110	pF
		Digital Inputs = V_{IL}			80	pF

ELECTRICAL CHARACTERISTICS (continued)

Parameter	Symbol	Conditions	DAC8043 Min	DAC8043 Typ	DAC8043 Max	Unit
TIMING CHARACTERISTICS[4, 14]						
Data Setup Time	t_{DS}	T_A = Full Temperature Range	40			ns
Data Hold Time	t_{DH}	T_A = Full Temperature Range	80			ns
Clock Pulsewidth High	t_{CH}	T_A = Full Temperature Range	90			ns
Clock Pulsewidth Low	t_{CL}	T_A = Full Temperature Range	120			ns
Load Pulsewidth	t_{LD}	T_A = Full Temperature Range	120			ns
LSB Clock Into Input Register to Load DAC Register Time	t_{ASB}	T_A = Full Temperature Range	0			ns
POWER SUPPLY						
Supply Voltage	V_{DD}		4.75	5	5.25	V
Supply Current	I_{DD}	Digital Inputs = V_{IH} or V_{IL}			500	µA max
		Digital Inputs = 0 V or V_{DD}			100	µA max

NOTES
[1] ±1/2 LSB = ±0.012% of full scale.
[2] All grades are monotonic to 12 bits over temperature.
[3] Using internal feedback resistor.
[4] Guaranteed by design and not tested.
[5] Applies to I_{OUT}; all digital inputs = 0 V.
[6] V_{REF} = 10 V; all digital inputs = 0 V.
[7] Calculated from worst-case R_{REF}: I_{ZSE} (in LSBs) = $(R_{REF} \times I_{LKG} \times 4096)/V_{REF}$.
[8] Absolute temperature coefficient is less than 300 ppm/°C.
[9] I_{OUT} load = 100 Ω, C_{EXT} = 13 pF, digital input = 0 V to V_{DD} or V_{DD} to 0 V. Extrapolated to 1/2 LSB; t_S = propagation delay (t_{PD}) + 9τ where τ = measured time constant of the final RC decay.
[10] V_{REF} = 0 V, all digital inputs = 0 V to V_{DD} or V_{DD} to 0 V.
[11] All digit inputs = 0 V.
[12] Calculations from en = $\sqrt{4K\ TRB}$ where: K = Boltzmann constant, J/°K, R = resistance, Ω, T = resistor temperature, °K, B = bandwidth, Hz.
[13] Digital inputs are CMOS gates; I_{IN} is typically 1 nA at 25°C.
[14] Tested at V_{IN} = 0 V or V_{DD}.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ V_{DD} = 5 V, V_{REF} = 10 V; I_{OUT} = GND = 0 V, T_A = 25°C.)

Parameter	Symbol	Conditions	DAC8043GBC Limit	Unit
STATIC ACCURACY				
Resolution	N		12	Bits min
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Gain Error	G_{FSE}	Using Internal Feedback Resistor	±2	LSB max
Power Supply Rejection Ratio	PSRR	ΔV_{DD} = ±5%	±0.002	%/% max
Output Leakage Current (I_{OUT})	I_{LKG}	Digital Inputs = V_{IL}	±5	nA max
REFERENCE INPUT				
Input Resistance	R_{IN}		7/15	kΩ min/max
DIGITAL INPUTS				
Digital Input HIGH	V_{IH}		2.4	V min
Digital Input LOW	V_{IL}		0.8	V max
Input Leakage Current	I_{IL}	V_{IN} = 0 V to V_{DD}	±1	µA max
POWER SUPPLY				
Supply Current	I_{DD}	Digital Inputs = V_{IN} or V_{IL}	500	µA max
		Digital Inputs = 0 V or V_{DD}	100	µA max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualifications through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS[1]
(T_A = 25°C, unless otherwise noted.)

V_{DD} to GND . . . . . –0.3 V to +8 V
V_{REF} to GND . . . . . ±18 V
V_{RFB} to GND . . . . . ±18 V
Digital Input Voltage Range . . . . . –0.3 V to V_{DD} + 0.3 V
V_{IOUT} to GND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
FP Versions . . . . . –40°C to +85°C
GP Version . . . . . 0°C to 70°C
Junction Temperature . . . . . 150°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 60 sec) . . . . . 300°C

Package Type	θ_{JA}[2]	θ_{JC}	Unit
8-Lead PDIP	96	37	°C/W

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.
[2]θ_{JA} is specified for worst-case mounting conditions, i. e., θ_{JA} is specified for device in socket for PDIP package.

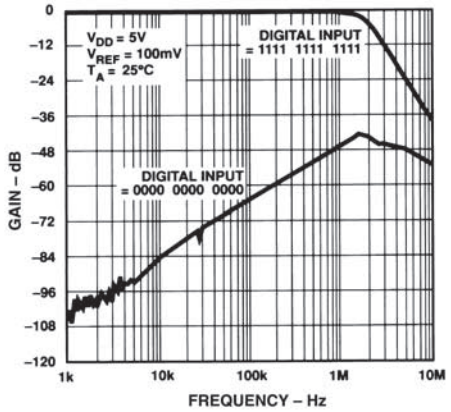
CAUTION
1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF} (Pin 1) and R_{FB} (Pin 2).
2. The digital control inputs are Zener-protected; however, permanent damage may occur on unprotected units from high energy electrostatic fields. Keep units in conductive foam at all times until ready to use.
3. Use proper antistatic handling procedures.
4. Absolute Maximum Ratings apply to both packaged devices and DICE. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device.

ORDERING GUIDE*

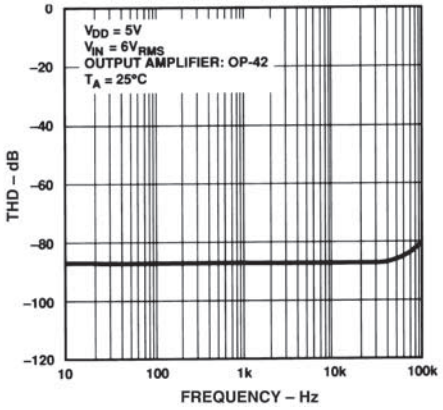
Model	Relative Accuracy	Temperature Range	Package Option
DAC8043FP	±1 LSB	–40°C to +85°C	8-Lead PDIP
DAC8043GP	±1/2 LSB	0°C to +70°C	8-Lead PDIP

*All commercial and industrial temperature range parts are available with burn-in.

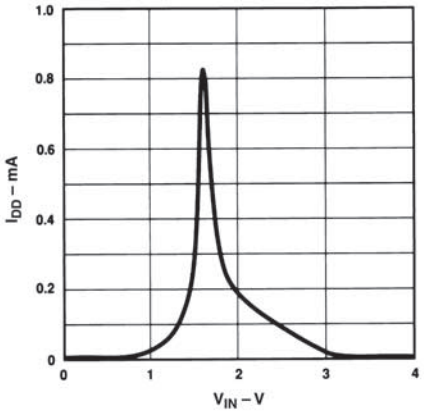
CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the DAC8043 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



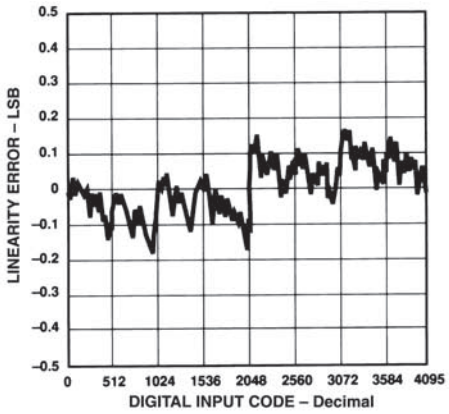
TPC 1. Gain vs. Frequency (Output Amplifier: OP42)



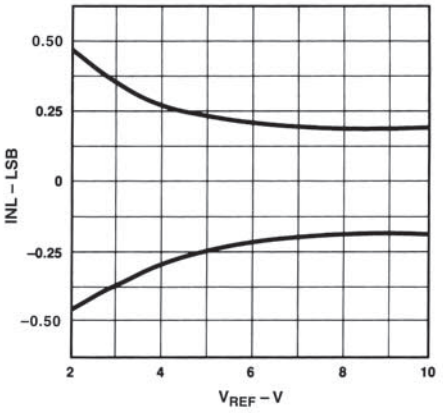
TPC 2. Total Harmonic Distortion vs. Frequency (Multiplying Mode)



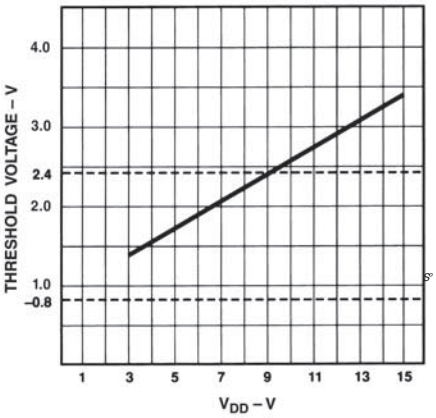
TPC 3. Supply Current vs. Logic Input Voltage



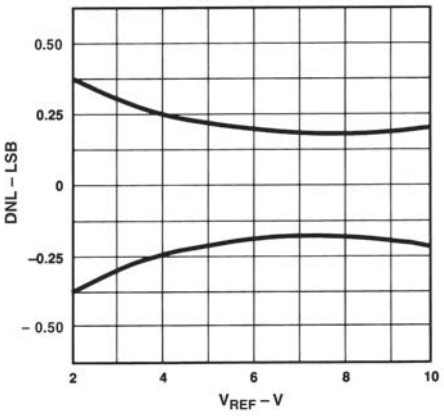
TPC 4. Linearity Error vs. Digital Code



TPC 5. Linearity Error vs. Reference Voltage



TPC 6. Logic Threshold Voltage vs. Supply Voltage



TPC 7. DNL Error vs. Reference Voltage

PARAMETER DEFINITIONS

Integral Nonlinearity (INL)

This is the single most important DAC specification. ADI measures INL as the maximum deviation of the analog output (from the ideal) from a straight line drawn between the end points. It is expressed as a percent of full-scale range or in terms of LSBs.

Refer to PMI 1988 Data Book Section 11 for additional digital-to-analog converter definitions.

Interface Logic Information

The DAC8043 has been designed for ease of operation. The timing diagram illustrates the input register loading sequence. Note that the most significant bit (MSB) is loaded first.

Once the input register is full, the data is transferred to the DAC register by taking $\overline{LD}$ momentarily low.

DIGITAL SECTION

The DAC8043's digital inputs, SRI, $\overline{LD}$, and CLK, are TTL compatible. The input voltage levels affect the amount of current drawn from the supply; peak supply current occurs as the digital input (V_{IN}) passes through the transition region (see TPC 3). Maintaining the digital input voltage levels as close as possible to the supplies, V_{DD} and GND, minimizes supply current consumption.

The DAC8043's digital inputs have been designed with ESD resistance incorporated through careful layout and the inclusion of input protection circuitry. Figure 1 shows the input protection diodes and series resistor; this input structure is duplicated on each digital input. High voltage static charges applied to the inputs are shunted to the supply and ground rails through forward biased diodes. These protection diodes were designed to clamp the inputs to well below dangerous levels during static discharge conditions.

GENERAL CIRCUIT INFORMATION

The DAC8043 is a 12-bit multiplying D/A converter with a very low temperature coefficient. It contains an R-2R resistor ladder network, data input, control logic, and two data registers.

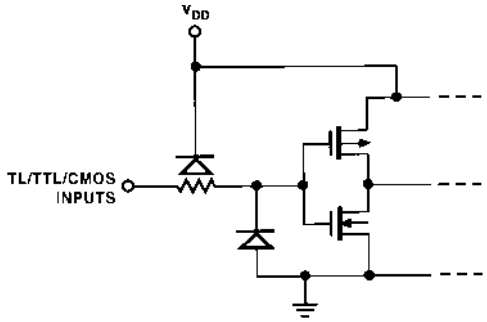


Figure 1. Digital Input Protection

The digital circuitry forms an interface in which serial data can be loaded under microprocessor control into a 12-bit shift register and then transferred, in parallel, to the 12-bit DAC register.

A simplified circuit of the DAC8043 is shown in Figure 3, which has an inverted R-2R ladder network consisting of silicon-chrome, highly stable (50 ppm/°C) thin-film resistors, and twelve pairs of NMOS current-steering switches.

These switches steer binarily weighted currents into either I_{OUT} or GND; this yields a constant current in each ladder leg, regardless of digital input code. This constant current results in a constant input resistance at V_{REF} equal to R. The V_{REF} input may be driven by any reference voltage or current, ac or dc, that is within the limits stated in the Absolute Maximum Ratings.

The twelve output current-steering NMOS FET switches are in series with each R-2R resistor; they can introduce bit errors if all are of the same R_{ON} resistance value. They were designed so that the switch ON resistance is binarily scaled so that the voltage drop across each switch remains constant. If, for example, Switch 1 of Figure 3 were designed with an ON resistance of 10 Ω, Switch 2 for 20 Ω, and so on, a constant 5 mV drop would be maintained across each switch.

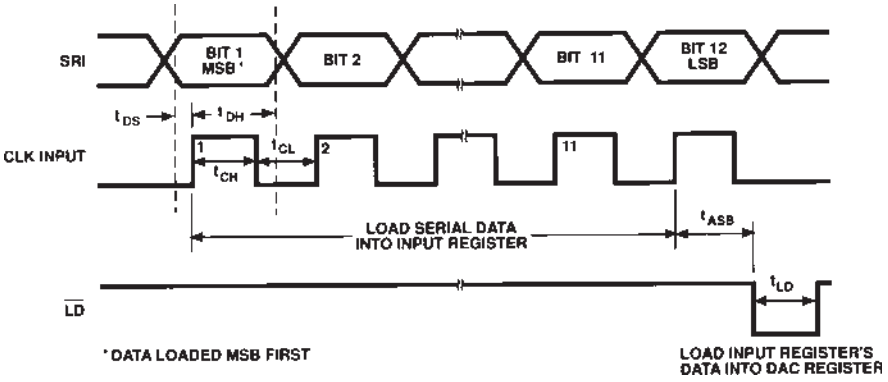


Figure 2. Write Cycle Timing Diagram

To further ensure accuracy across the full temperature range, permanently ON MOS switches were included in series with the feedback resistor and the R-2R ladder's terminating resistor. The simplified DAC circuit, Figure 3, shows the location of the series switches. These series switches are equivalently scaled to two times Switch 1 (MSB) and to Switch 12 (LSB), respectively, to maintain constant relative voltage drops with varying temperature. During any testing of the resistor ladder or $R_{FEEDBACK}$ (such as incoming inspection), V_{DD} must be present to turn ON these series switches.

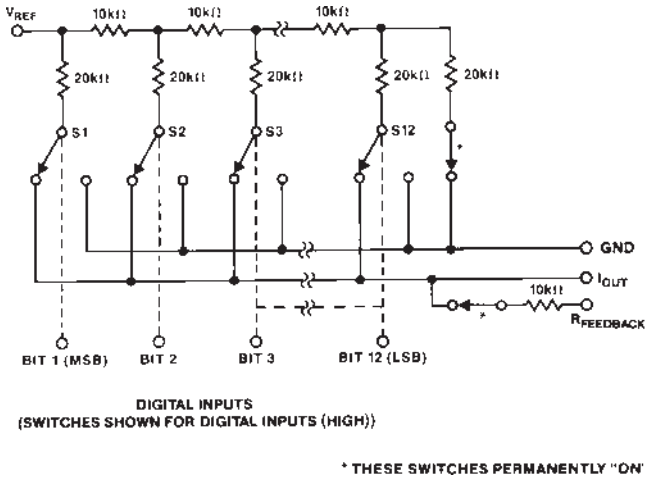


Figure 3. Simplified DAC Circuit

EQUIVALENT CIRCUIT ANALYSIS

Figure 4 shows an equivalent analog circuit for the DAC8043. The $(D \times V_{REF})/R$ current source is code dependent and is the current generated by the DAC. The current source I_{LKG} consists of surface and junction leakages and doubles approximately every 10°C. C_{OUT} is the output capacitance; it is the result of the N-channel MOS switches and varies from 80 pF to 110 pF, depending on the digital input code. R_O is the equivalent output resistance that also varies with digital input code. R is the nominal R-2R resistor ladder resistance.

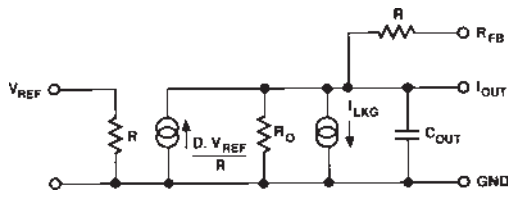


Figure 4. Equivalent Analog Circuit

DYNAMIC PERFORMANCE

Output Impedance

The DAC8043's output resistance, as in the case of the output capacitance, varies with the digital input code. This resistance, looking back into the I_{OUT} terminal, may be between 10 kΩ (the feedback resistor alone when all digital inputs are low) and 7.5 kΩ (the feedback resistor in parallel with approximately 30 kΩ of the R-2R ladder network resistance when any single bit logic is high). Static accuracy and dynamic performance will be affected by these variations. This variation is best illustrated by using the circuit of Figure 5 and the equation

$$V_{ERROR} = V_{OS}\left(1 + \frac{R_{FB}}{R_O}\right)$$

where R_O is a function of the digital code and

R_O = 10 kΩ for more than four bits of Logic 1
R_O = 30 kΩ for any single bit of Logic 1

Therefore, the offset gain varies as follows:

at code 0011 1111 1111,

$$V_{ERROR1} = V_{OS}\left(1 + \frac{10\ k\Omega}{10\ k\Omega}\right) = 2\,V_{OS}$$

at code 0100 0000 0000,

$$V_{ERROR2} = V_{OS}\left(1 + \frac{10\ k\Omega}{30\ k\Omega}\right) = 4/3\,V_{OS}$$

The error difference is 2/3 V_{OS}.

Since one LSB has a weight (for V_{REF} = 10 V) of 2.4 mV for the DAC8043, it is clearly important that V_{OS} be minimized, either by using the amplifier's nulling pins or an external nulling network or by selecting an amplifier with inherently low V_{OS}. Amplifiers with sufficiently low V_{OS} include ADI's OP77, OP07, OP27, and OP42.

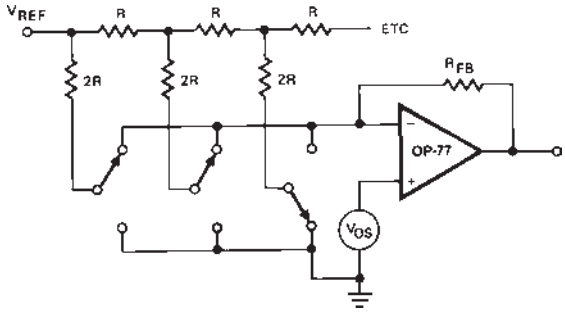


Figure 5. Simplified Circuit

The gain and phase stability of the output amplifier, board layout, and power supply decoupling all affect the dynamic performance. The use of a small compensation capacitor may be required when high speed operational amplifiers are used. It may be connected across the amplifier's feedback resistor to provide the necessary phase compensation to critically damp the output. The DAC8043's output capacitance and the R_{FB} resistor form a pole that must be outside the amplifier's unity gain crossover frequency.

The considerations when using high speed amplifiers are:

1. Phase compensation (see Figures 6 and 7).
2. Power supply decoupling at the device socket and the use of proper grounding techniques.

APPLICATIONS INFORMATION

Application Tips

In most applications, linearity depends upon the potential of I_{OUT} and GND (Pins 3 and 4) being equal to each other. In most applications, the DAC is connected to an external op amp with its noninverting input tied to ground (see Figures 6 and 7). The amplifier selected should have a low input bias current and low drift over temperature. The amplifier's input offset voltage should be nulled to less than 200 µV (less than 10% of 1 LSB).

The operational amplifier's noninverting input should have a minimum resistance connection to ground; the usual bias current compensation resistor should not be used. This resistor can cause a variable offset voltage appearing as a varying output error. All grounded pins should tie to a single common ground point, avoiding ground loops. The V_{DD} power supply should have a low noise level with no transients greater than 17 V.

Unipolar Operation (2-Quadrant)

The circuit shown in Figures 6 and 7 may be used with an ac or dc reference voltage. The circuit's output will range between 0 V and approximately $-V_{REF}$ (4095/4096), depending upon the digital input code. The relationship between the digital input and the analog output is shown in Table I. The limiting parameters for the V_{REF} range are the maximum input voltage range of the op amp or ±25 V, whichever is lowest.

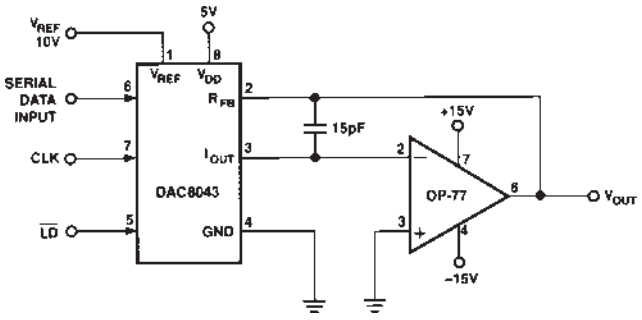


Figure 6. Unipolar Operation with High Accuracy Op Amp (2-Quadrant)

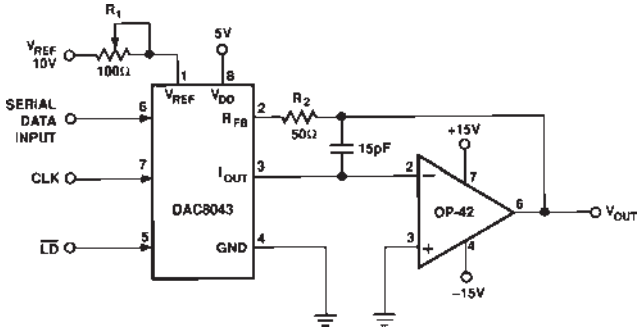


Figure 7. Unipolar Operation with Fast Op Amp and Gain Error Trimming (2-Quadrant)

Gain error may be trimmed by adjusting R_1, as shown in Figure 7. The DAC register must first be loaded with all 1s. R_1 may then be adjusted until $V_{OUT} = -V_{REF}$ (4095/4096). In the case of an adjustable V_{REF}, R_1 and R_2 may be omitted, with V_{REF} adjusted to yield the desired full-scale output.

In most applications, the DAC8043's negligible zero-scale error and very low gain error permit the elimination of the trimming components (R_1 and the external R_2) without adversely affecting on circuit performance.

Table I. Unipolar Code Table

Digital Input MSB LSB	Nominal Analog Output (V_{OUT} as Shown in Figures 6 and 7)
1111 1111 1111	$-V_{REF}\left(\frac{4095}{4096}\right)$
1000 0000 0001	$-V_{REF}\left(\frac{2049}{4096}\right)$
1000 0000 0000	$-V_{REF}\left(\frac{2048}{4096}\right) = -\frac{V_{REF}}{2}$
0111 1111 1111	$-V_{REF}\left(\frac{2047}{4096}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{1}{4096}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{0}{4096}\right) = 0$

NOTES

1. Nominal full scale for Figures 6 and 7 circuits is given by

$$FS = -V_{REF}\left(\frac{4095}{4096}\right)$$

2. Nominal LSB magnitude for Figures 6 and 7 circuits is given by

$$LSB = V_{REF}\left(\frac{1}{4096}\right) or\ V_{REF}\left(2^{-n}\right)$$

Table II. Bipolar (Offset Binary) Code Table

Digital Input MSB LSB	Nominal Analog Output (V_{OUT} as Shown in Figure 8)
1111 1111 1111	$+V_{REF}\left(\frac{2047}{2048}\right)$
1000 0000 0001	$+V_{REF}\left(\frac{1}{2048}\right)$
1000 0000 0000	0
0111 1111 1111	$-V_{REF}\left(\frac{1}{2048}\right)$
0000 0000 0001	$-V_{REF}\left(\frac{2047}{2048}\right)$
0000 0000 0000	$-V_{REF}\left(\frac{2048}{2048}\right)$

NOTES
1. Nominal full scale for Figure 8 circuit is given by

$$FS = V_{REF}\left(\frac{2047}{2048}\right)$$

2. Nominal LSB magnitude for Figure 8 circuit is given by

$$LSB = V_{REF}\left(\frac{1}{2048}\right)$$

Bipolar Operation (4-Quadrant)
Figure 8 details a suggested circuit for bipolar, or offset binary, operation. Table II shows the digital input to analog output relationship. The circuit uses offset binary coding. Twos complement code can be converted to offset binary by software inversion of the MSB or by the addition of an external inverter to the MSB input.

Resistors R_3, R_4, and R_5 must be selected to match within 0.01%, and they all must be of the same (preferably metal foil) type to ensure temperature coefficient matching. Mismatching between R_3 and R_4 causes offset and full-scale errors, while an R_5 to R_4 and R_3 mismatch will result in full-scale error.

Calibration is performed by loading the DAC register with 1000 0000 0000 and adjusting R_1 until V_{OUT} = 0 V. R_1 and R_2 may be omitted, adjusting the ratio of R_3 to R_4 to yield V_{OUT} = 0 V. Full scale can be adjusted by loading the DAC register with 1111 1111 1111 and either adjusting the amplitude of V_{REF} or the value of R_5 until the desired V_{OUT} is achieved.

Analog/Digital Division
The transfer function for the DAC8043 connected in the multiplying mode, as shown in Figures 6, 7, and 8, is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^{12}}\right)$$

where A_X assumes a value of 1 for an ON bit and 0 for an OFF bit.

The transfer function is modified when the DAC is connected in the feedback of an operational amplifier, as shown in Figure 9 and becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \ldots \frac{A_{12}}{2^4}}\right)$$

The above transfer function is the division of an analog voltage (V_{REF}) by a digital word. The amplifier goes to the rails with all bits OFF since division by zero is infinity. With all bits ON the gain is 1 (±1 LSB). The gain becomes 4096 with the LSB, bit 12, ON.

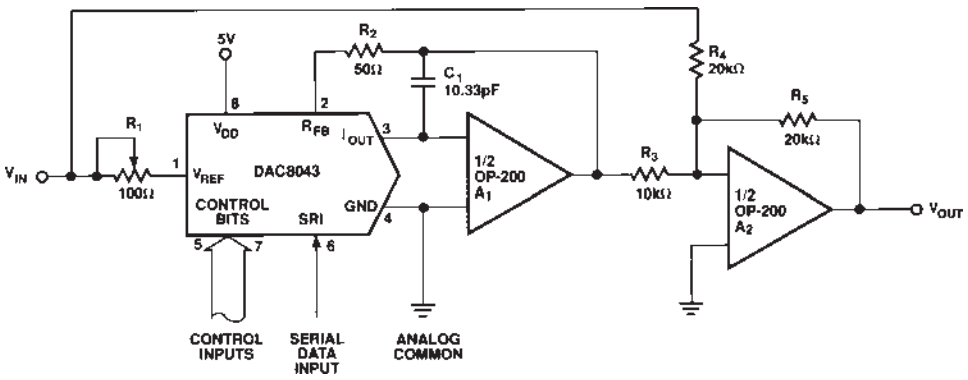


Figure 8. Bipolar Operation (4-Quadrant, Offset Binary)

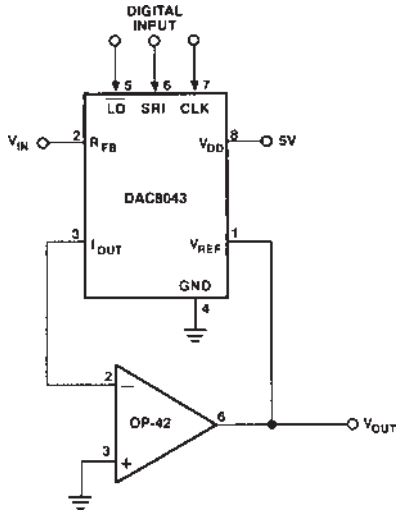


Figure 9. Analog/Digital Divider

Interfacing to the MC6800

As shown in Figure 10, the DAC8043 may be interfaced to the 6800 by successively executing memory WRITE instructions while manipulating the data between WRITEs, so that each WRITE presents the next bit.

In this example the most significant bits are found in memory location 0000 and 0001. The four MSBs are found in the lower half of 0000, the eight LSBs in 0001. The data is taken from the DB_7 line.

The serial data loading is triggered by the CLK pulse, which is asserted by a decoded memory WRITE to memory location 2000, R/$\overline{W}$, and ϕ2. A WRITE to address 4000 transfers data from the input register to the DAC register.

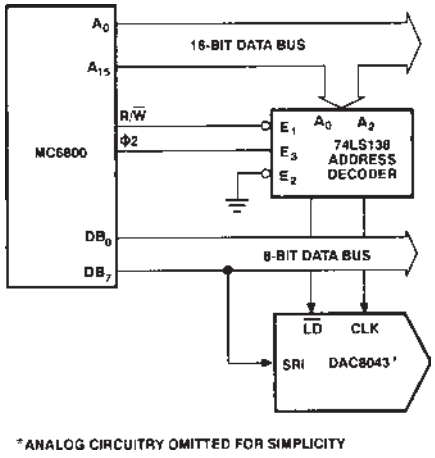


Figure 10. DAC8043 to MC6800 Interface

DAC8043 Interface to the 8085

The DAC8043's interface to the 8085 microprocessor is shown in Figure 11. Note that the microprocessor's SOD line is used to present data serially to the DAC.

Data is clocked into the DAC8043 by executing memory WRITE instructions. The clock input is generated by decoding address 8000 and $\overline{WR}$. Data is loaded into the DAC register with a memory write instruction to address A000.

Serial data supplied to the DAC8043 must be present in the right justified format in Registers H and L of the microprocessor.

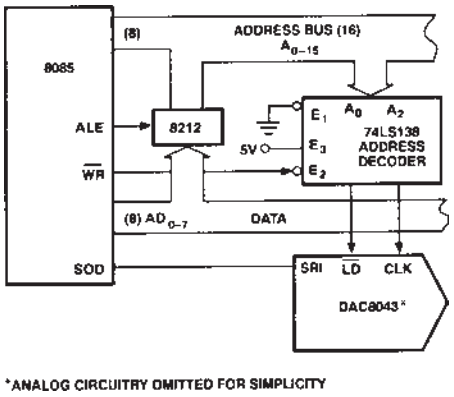


Figure 11. DAC8043 to 8085 Interface

DAC8043 to the 68000 Interface

The DAC8043 interfacing to the 68000 microprocessor is shown in Figure 12. Again, serial data to the DAC is taken from one of the microprocessor's data bus lines.

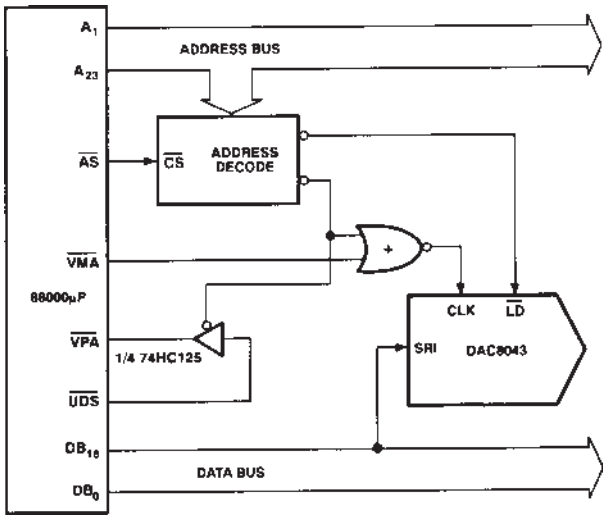
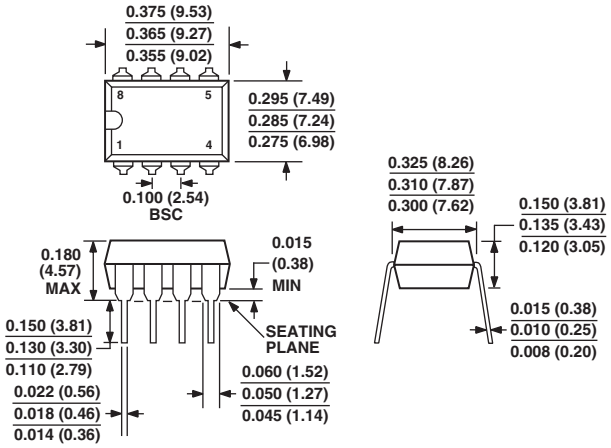


Figure 12. DAC8043 to 68000 μP Interface

OUTLINE DIMENSIONS

8-Lead Plastic Dual In-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
3/03—Data Sheet changed from REV. C to REV. D.	
Deleted 8-Lead CIRDIP and 16-Lead Wide-Body SOL	Universal
Figures renumbered	Universal
Changes to ABSOLUTE MAXIMUM RATINGS	4
Changes to ORDERING GUIDE	4
Deleted to DICE CHARACTERISTICS	4
Updated OUTLINE DIMENSIONS	11

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